PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

S. SAITO

Group Art Unit: Unknown

Application No.: Not Yet Assigned

Examiner: Unknown

Filed: Concurrently Herewith

Attorney Dkt. No.: 024016-00020

For: PLL FREQUENCY SYNTHESIZER

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

December 27, 2001

Sir:

Prior to initial examination of the application, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 8, lines 22 and 23

Fig. 5A and 5B are circuit diagrams illustrating specific examples of a low-pass filter (LPF) circuit employed in the second embodiment;

Page 8, line 30 and Page 9, line 1

Fig. 9A, 9B and 9C are circuit diagrams showing specific examples of a charge pump circuit employed in the fourth embodiment;

Page 9, lines 2 and 3

Fig. 10A and 10B are circuit diagrams depicting a specific example of a low-pass filter (LPF) circuit;

REMARKS

The above amendments to the specification have been made in order to place the Brief Description of the Drawings in the specification into conformance with the drawings being filed with the application.

Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300.

Respectfully submitted,

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The above and further objects and novel features of the invention will more fully appear from following detailed description when the same is read in connection with the accompanying drawings. It is to be expressly understood, however, that the drawings are for the purpose of illustration only and are not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of this specification illustrate an embodiment of the invention and, together with the description, serve to explain the objects, advantages and principles of the invention.

In the drawings,

FIG. 1 is a function block diagram showing a PLL frequency synthesizer according to a first embodiment of the present invention;

FIG. 2 is a waveform diagram illustrating operating waveforms of the PLL frequency synthesizer according to the first embodiment;

FIG. 3 is a function block diagram depicting a specific example of the PLL frequency synthesizer according to the first embodiment;

FIG. 4 is a function block diagram showing a PLL frequency synthesizer according to a second embodiment of the present invention;

FIG. 5 is a circuit diagram illustrating specific examples of a low-pass filter (LPF) circuit employed in the second embodiment;

FIG. 6 is a function block diagram depicting a PLL frequency synthesizer according to a third embodiment of the present invention;

FIG. 7 is a circuit diagram showing a specific example of a low-pass filter (LPF) circuit employed in the third embodiment;

FIG. 8 is a function block diagram illustrating a PLL frequency synthesizer according to a fourth embodiment of the present invention;

FIG. 9 is a circuit diagram showing specific examples of a charge

pump circuit employed in the fourth embodiment;

FIG. 10 is a circuit diagram depicting a specific example of a low-pass filter (LPF) circuit;

FIG. 11 is a function block diagram showing a PLL frequency synthesizer according to a prior art;

FIG. 12 is a waveform diagram illustrating operating waveforms of the PLL frequency synthesizer according to the prior art; and

FIG. 13 is a characteristic diagram showing input/output characteristics of a charge pump circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

First through fourth embodiments in which PLL frequency synthesizers of the present invention have been embodied respectively, will hereinafter be described in detail with reference to the accompanying drawings based on FIGS. 1 through 10.

A PLL frequency synthesizer according to a first embodiment shown in FIG. 1 has a configuration wherein a switch circuit 10 controlled by a control signal Scnt is interposed between a low-pass filter (LPF) circuit 103 and a voltage-controlled oscillator (VCO) 104 in addition to the function block diagram showing the prior art shown in FIG. 11. In the present embodiment, respective components of a phase comparator 101, a charge pump circuit 102, a low-pass filter (LPF) circuit 103 and a voltage-controlled oscillator (VCO) 104 are similar to the prior art shown in FIG. 11 in their configurations, operations and effects. Further, the configuration of the PLL frequency synthesizer 1 wherein a frequency signal fp outputted from the voltage-controlled oscillator (VCO) 104 is fed back to the phase comparator 101 so as to constitute a feedback loop, is also similar to the prior art shown in FIG. 11.

In the first embodiment illustrated in FIG. 1, the switch circuit